Remarks

Reexamination and reconsideration of this application is requested. Claims 1, 3, 6 and 18 have been amended in this Response. Claims 2, 4, 5, and 9 have been cancelled. Claims 1, 3, 6, 7, 8, 10-34 remain in the application.

Specification

The disclosure was objected to because of informalities in the specification. The following changes on pages 1, 4 and 5 of the specification are to satisfy the Examiner's required changes.

Please replace the first paragraph in the BACKGROUND section on page 1, starting on line 6, with the following paragraph:

Today's portable communication products utilize circuits that may perform a variety of applications. Some of the new applications are user defined and the more complex applications are even down-loadable. A product's marketplace success may depend on a continual stream of upgrades and modified applications to enrich a product's features and functionality. At the same time, the user expects the products to include high data rate capabilities, sometimes at a reduced product size and cost.

Please replace the paragraph on page 4, starting on line 23, with the following paragraph:

Applications processor 12 and baseband processor 16 may communicate with one another over fourteen signal paths or connections, although this is not a limitation of the present invention. The fourteen signal paths that connect port 14 and port 18 may be thought of as two sets of signal paths. The first set of signal paths (inbound signals) between TX control 28 and RX control 48 include the signals CLOCK, STROBE, WAIT and the data signals DATA 0, DATA 1, DATA 2 and DATA 3. The second set of signal paths (outbound signals) between RX control 38 and TX control 58 also include the additional signals CLOCK, STROBE, WAIT and the data signals DATA 0, DATA 1, DATA 2 and DATA 3. The same signal names signify that the same type of signal may be transferred over the signal path. For instance, in the first set the data signals DATA 0, DATA 1, DATA 2 and DATA 3 may be transferred on signal paths from TX control 28 to RX control 48 and in the second set the data signals DATA 0, DATA 1, DATA 2 and DATA 3 may be transferred on signal paths

from TX control 58 to RX control 38. In this particular embodiment, there are four outbound data signal paths and four inbound data signal paths, but the number of inbound and outbound signal paths is not intended as a limitation of the present invention.

Please replace the paragraph on page 5, starting on line 10, with the following paragraph:

A storage register or configuration register 21 in control registers 22 and a configuration register 41 in control registers 42 may be programmed, and thus, define the flow of data across interface 20. By programming configuration register 21, the number of signal paths that actively transfer data from TX control 28 to RX control 48 may be modified. The value of two bits of a data field in configuration register 21 may control the number of data signals DATA 0, DATA 1, DATA 2 and DATA 3 that are active. In other words, configuration register 21 may set all of the data signal paths to transfer data, some of the data signal paths to transfer data or none of the data signal paths to transfer data. Put another way, a portion of the signal paths between port 14 and port 18 may be programmed, as determined by the data in the data fields of the configuration registers, to become inactive. Similarly, by programming configuration register 41, the number of signal paths that actively transfer data from TX control 58 to RX control 38 may be modified. In accordance with one embodiment of the present invention, a register field of two-bits in configuration register 41 may control which of the signal paths that transfer the data signals DATA 0, DATA 1, DATA 2 and DATA 3 are active and which are inactive. Although configuration register 21 and configuration register 41 have been described as registers, the method for storing the data field value is not limited in this respect. Other embodiments of the present invention may use other methods such as a memory or latches for storing data in the register field.

A marked-up copy of these three paragraphs is included in Appendix A of this amendment.

Response to 35 U.S.C. §112 and 35 U.S.C. §102 (b) Rejection

The Office Action rejects claims 1 and 6 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1 and 6 have been amended to remove the word "channel", and in so doing, the amended claims are believed to overcome the 35 U.S.C. §112, second paragraph, rejection. Further, the Examiner has indicated that the prior art fails to teach or suggest a strobe signal, wherein an identity of the channel is provided during the strobe signal. Claims 1 and 6 have been amended to include this limitation and are now believed to be novel.

Claim 3 depends from base claim 1 and claims 7 and 8 depend from base claim 6 and are believed to be allowable for at least the same reasons as base claims 1 and 6.

Response to the 35 U.S.C. §102 (b) Rejection

The Office Action rejects claims 10, 11, 16, 17, 27 and 32 under 35 U.S.C. §102 (b) as being anticipated by Krasner having U.S. Patent No. 5,663,734.

Applicant's claim 10 recites, among other things, a first processor having a first set of terminals for outbound data and a second set of terminals for inbound data and including a register having a data field to determine the terminals in the first set that provide outbound data.

Applicant respectfully disagrees with the Examiner that Krasner shows the features and limitations of base claim 10. First, Krasner shows in FIG. 1A a microprocessor 26 that receives a first Input/Output (I/O) bus 33 connected to DSP chip 32, a second I/O bus 35 connected to a FPGA 48 and a serial I/O bus 25 connected to modem 22. Applicant's claim 10 clearly states that a first microprocessor has a first set of terminals to provide outbound data and a second set of terminals for inbound data. Whereas Krasner describes I/O terminals, Applicant claims a first processor having a first set of terminals for inputs and a second set of terminals for outputs, with both the first and second sets of terminals coupled to a second microprocessor. It is respectfully pointed out that only on set of terminals, i.e., bus 33, connects processor 32 to microprocessor 26, and this set of terminals

are I/O terminals. Thus, Krasner teaches I/O buffers having one common set of terminals to handle both inputs and outputs and not separate sets of terminals as claimed in Applicant's claim 10.

Second, Applicant claims a register having a data field to determine the terminals in the first set that provide outbound data. Applicant respectfully disagrees that microprocessor 26 has such a register. Instead, the bi-directional buses 33 and 35 are configured as either ALL inputs or ALL outputs. Although not shown in detail, the direction of the I/O buffers is most likely based on a Read/Write control signal, a signal that is not stored in a register as suggested by the Examiner. With reference to Krasner's FIG. 1A, Applicant respectfully points out that neither the Read/Write control signal, nor any other control signal, selects terminals in the first set to provide outbound data as claimed in Applicant's claim 10.

Accordingly, Since Krasner does not illustrate or discuss terminals in a first set that provide outbound data and terminals in a second set that provide inbound data, with a register having a data field to determine the terminals in the first set that provide outbound data, the relied upon reference cannot anticipate Applicant's claim 10.

Claims 11, 16 and 17 depend from base claim 10 and are believed to be allowable over the prior art reference of Krasner for at least the same reasons as base claim 10.

Response to the 35 U.S.C. §102 (b) Rejection

The Office Action rejects claims 18 and 19 under 35 U.S.C. §102 (b) as being anticipated by Nakano et al. having U.S. Patent No. 5,663,734.

Applicant's base claim 18 has been amended to recite "a terminal to provide a strobe signal, wherein an identity of a register to output data is provided at the data terminals during the strobe signal." It is believed that the amended claim language overcomes the prior art references and that claim 18, along with dependent claims 19-22, are allowable.

Response to the 35 U.S.C. §102 (b) Rejection

The Office Action rejects claims 27 and 32 under 35 U.S.C. §102 (b) as being anticipated by Krasner.

Applicant's claim 27 recites transferring data from an applications processor to a baseband processor through a first set of data pins and transferring data from the baseband processor to the applications processor through a second set of data pins.

As previously mentioned, Krasner teaches two microprocessors, i.e., DSP chip 32 and microprocessor 26. FIG. 1A shows that microprocessor 26 is connected via an Input/Output (I/O) bus 33 to DSP chip 32. Applicant's claim 27 clearly states when data is transferred from the applications processor to the baseband processor that a first set of data pins is used, and that when data is transferred from the baseband processor to the applications processor a second set of data pins is used. Note that Krasner describes only one I/O bus, i.e., a bi-directional single set of terminals, and not separate first and second sets of terminals connected between the baseband processor and the applications processor as claimed in Applicant's claim 27. Accordingly, the prior art of Krasner cannot anticipate Applicant's claim 27.

Similarly, Applicant's claim 32 recites, (a) transferring data from an applications processor to a baseband processor through a first set of data pins; and (b), transferring data from the baseband processor to the applications processor through a second set of data pins. Again, Krasner teaches only a bi-directional single set of I/O terminals and cannot anticipate Applicant's separate first and second sets of terminals connected between the baseband processor and the applications processor as claimed in Applicant's claim 32.

Response to the 35 U.S.C. §103 (a) Rejection

The Office Action rejects claims 12-15 under 35 U.S.C. §103 (a) as being unpatentable over Krasner in view of Nakano and Xilinx.

The Examiner states that Krasner discloses the system of claim 10. As previously stated, Applicant respectfully disagrees with the Examiner. Krasner discloses first and second processors connected only by an I/O bus 33. Krasner does not disclose a first processor having a first set of terminals for outbound data

and a second set of terminals for inbound data. Neither does Krasner disclose a second processor having a first set of terminals for inbound data that are coupled to the first set of terminals of the first processor, and a second set of terminals for outbound data that are coupled to the second set of terminals of the first processor. Since Krasner, Nakano, Xilinx, either singularly or in combination, do not teach or suggest all of the features and limitations of Applicant's base claim, claims 12-15 that depend from base claim 10 are believed allowable over the art of record.

Response to the 35 U.S.C. §103 (a) Rejection

The Office Action rejects claims 28-31, 33 and 34 under 35 U.S.C. §103 (a) as being unpatentable over Krasner in view of Nakano and Xilinx.

Claims 28-31 depend from base claim 27 and claims 33 and 34 depend from base claim 32. Base claims 27 and 32 are believed allowable over the prior art of record for reasons stated above. Accordingly, dependent claims 28-31 and 33-34 are believed allowable for at least the same reasons as the base claims.

Allowed Claims

Applicants would like to gratefully acknowledge the Examiner's indication that claims 23-26 are allowable and that claims 2-5 and 9 would be allowable if the objection as being dependent upon a rejected base claim were overcome. As already shown in the amended claims, the limitations of the allowable dependent claims have been incorporate into Applicant's independent claims.

Conclusion

The foregoing is submitted as a full and complete response to the Office Action mailed September 22, 2003, and it is submitted that claims 1, 3, 6, 7, 8, 10-34 are in condition for allowance. Reconsideration of the rejection is requested. Allowance of these claims is earnestly solicited.

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Should it be determined that an additional fee is due under 37 CFR §1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account #50-0221.

If the Examiner believes that there are any informalities that can be corrected by an Examiner's amendment, a telephone call to the undersigned at (480) 552-1388 is respectfully solicited.

Respectfully submitted,
Scott C. Glenn

Lanny L. Parker
Patent Agent
Reg. No. 44,281

c/o Blakely, Sokoloff, Taylor & Zafman, LLP
12400 Wilshire Blvd., Seventh Floor
Los Angeles, CA 90025-1026
(503) 264-0967

Appendix A

This marked-up paragraph shows the changes to the paragraph found on page 1, line 6.

Today's portable communication products utilize circuits that may perform a variety of applications. Some of the new applications are user defined and the more complex applications are even ~~down-loadable~~ down-loadable. A product's marketplace success may depend on a continual stream of upgrades and modified applications to enrich a product's features and functionality. At the same time, the user expects the products to include high data rate capabilities, sometimes at a reduced product size and cost.

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